



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,323	03/29/2004	Ahmad R. Ansari	NEC0217C2US	2725
33031 7590 06/07/2007 CAMPBELL STEPHENSON ASCOLESE, LLP 4807 SPICEWOOD SPRINGS RD. BLDG. 4, SUITE 201 AUSTIN, TX 78759			EXAMINER ELLIS, RICHARD L	
			ART UNIT 2183	PAPER NUMBER
			MAIL DATE 06/07/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/812,323	ANSARI, AHMAD R.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 22 May 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 28-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 28-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

1. Claims 28-41 are presented for examination.
2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

5. Claims 28 and 31 are rejected under 35 USC § 102(e) as being clearly anticipated by Shu et al., U.S. Patent 5,928,350.

Shu et al. taught (e.g. see figs. 1-5) the invention as claimed (as per claim 28), including a data processing ("DP") system comprising:

- A. a method comprising issuing an instruction (col. 4 lines 30-33, presence of "instruction" execution blocks indicate that the system had the ability to issue instructions and that these instructions would have caused data transfers to/from memory to occur. Furthermore see fig. 1 which shows both read and write to/from memory for execution of instructions.) to transfer data between a memory (fig. 5, 72) and a processor (36);
- B. wherein the data comprises a plurality of data elements each having a data width (col. 8 lines 36-40, 32 bits);

- C. transferring the data between the memory and the processor via a memory bus coupled therebetween (74);
  - D. wherein the data is transferred two or more data elements at a time (col. 8 lines 40-44, nine items of 32 bits transferred at a time, nine being greater than two).
- 6.

As to claim 31, Shu et al. taught transferring the data to be transferred between the memory and the processor via a burst transfer (in Shu et al.'s embodiment, a burst of nine items).

7. Claims 33 and 39 are rejected under 35 USC 102(b) as being clearly anticipated by Getzlaff et al., IBM Technical Disclosure Bulletin, Vol. 38, No. 5, May 1995.

Getzlaff et al. taught (e.g. see figs. 1-2) the invention as claimed (as per claim 33), including a data processing ("DP") system comprising:

- A. a computer readable medium comprising instructions executable by a computer system (pg. 409, lines 18-19, Getzlaff et al. discloses "an instruction" and therefore inherently discloses a "computer readable medium" in order for that instruction to recognize its functionality in a computer system);
  - B. wherein the computer system which performs a method comprising determining a quantity of data elements to be transferred in parallel between a memory and a processor via a memory bus coupled therebetween, wherein the quantity is determined from a width of the data elements to be transferred and a width of the memory bus (pg. 409, lines 19-24);
  - C. initiating a transfer of the quantity of data elements between the memory and the processor (pg. 409, lines 19-24, the discussion talks about "transferring" and "accessing" and therefore indicates that the transfer specified is "initiated").
8. As to claim 39, Getzlaff et al. taught the invention as discussed in the rejection of claim 33, supra. Getzlaff et al. additionally taught a memory (pg. 407, line 3, "virtual storage"), a processor (pg. 407, line 1, "CISC computer architectures") and a circuit (fig. 2).

9. Claims 29 and 32 are rejected under 35 USC § 103 as being unpatentable over Shu et al., U.S. patent 5,928,350, as applied to claim 28, supra., in view of Smith, U.S. Patent 5,895,501.

Smith was cited as a prior art reference in paper number 20060905, mailed 9/6/2006.

10. As to claim 29, Shu et al. did not teach determining an ending address of data to be transferred from a starting address and data width, and generation of an address exception when it was determined that the data to be transferred crossed a page boundary of a page in memory.

Smith taught determining an ending address from a starting address and data width (col. 7 lines 58-62, where the "vector length" is the size of the data being operated upon by the memory bus because it defines the size of the vector being loaded or stored) and generate of an address exception when it was determined that the data to be transferred crossed a page boundary (col. 7 line 58 to col. 8 line 8).

11. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined the teachings of Smith with Shu et al. because of Smith's teaching that in vector processing systems (col. 1 lines 11-15) there are special memory needs (col. 2 lines 55-60) including a need to determine page boundary crossing early in order to maintain performance (col. 3 lines 22-30).

12. As to claim 32, Smith taught interrupting the data transfer in response to generating the address exception (col. 7 lines 50-65).

13. Claim 30 is rejected under 35 USC § 103 as being unpatentable over Shu et al. in view of Smith as applied to claim 29, supra. Additionally Andrew Koenig, *C Traps and Pit Falls*, 1988 is cited as evidence showing the calculation of the size of a vector in memory.

14. As to claim 30, applicant has simply claimed a mere mathematical algorithm, that algorithm being the basic, obvious, method of calculating the address of the last one of a list of plural elements, each of size X, with a stride between elements of size Y. As seen from Koenig, on pg. 28, to calculate the size of a vector in memory one multiplies the number of elements by the individual size of each element ( "sizeof(calendar) is 372 (31x12) times

sizeof(int)" ). This calculation provides the total size of the vector in memory. If this size is then summed with the starting address, the result will obviously be the next address past the vector. Therefore, by simple mathematical deduction, in order to locate the address of the final element in memory, one simply calculates the size of the vector minus one element. This value, when summed with the starting address will then refer to the final element in memory. As applicant's claims recite finding the "ending address of the data" applicant is locating the address of the end (last one) of the data, and not the address of the next location past the data set. Therefore, through simple mathematical deduction, it would have been obvious to one of ordinary skill in the art at the time the invention was made to subtract one from the length before multiplying by the width and stride and length in order to arrive at the address of the last one of the data elements.

15. Claims 34-37 and 40-41 are rejected under 35 USC § 103 as being unpatentable over Getzlaff et al. Additionally Andrew Koenig, *C Traps and Pit Falls*, 1988 is cited as evidence showing the calculation of the size of a vector in memory. Getzlaff et al. taught generation of an exception with it was determined that data to be transferred crossed a page boundary of a page in the memory (pg. 409, lines 24-25). Getzlaff et al. did not teach determining a vector ending address as claimed. However, as explained in the rejection of claim 30, supra, applicant has merely claimed the obvious mathematical operation to compute the ending address of a vector of data.
16. As to claim 36, Getzlaff et al. taught transferring the data via a burst transfer (pg. 409, lines 18-25, Getzlaff et al. prefers bursts of 4 bytes in size).
17. As to claim 37, Getzlaff et al. taught interrupting the data transfer in response to generating an address exception (pg. 409, lines 24-25).
18. Claim 38 is rejected under 35 USC § 103 as being unpatentable over Getzlaff et al., in view of Porter et al., U.S. patent 4,268,907.  
As to claim 38, Getzlaff et al. did not teach cache bypassing as claimed. However, Proter et al. taught cache bypassing as claimed (col. 2 lines 35-63).

19. It would have been obvious to one of ordinary skill in the art to have combined the teachings of Ketzlaff et al. with Porter et al. because of Porter et al.'s teaching that movement of large data blocks is equivalent to a cache flush (col. 2 lines 13-19) that result in a performance degradation (col. 2 lines 27-32) and that by preventing caching of such operations, the performance degradation is avoided (col. 2 lines 27-32, col. 2 line 64 to col. 3 line 27).

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

IBM TDB, "Method for Handling Unaligned Operands that Extend Across Memory Protection Boundaries in a Microprocessor", April 1994.

US Patents 6,330,623, Re. 36,052, 5,255,378, and 5,911,151.

All of the above references are pertinent because they also disclose use of a memory bus width in the calculation of an amount of data to transfer on the memory bus.

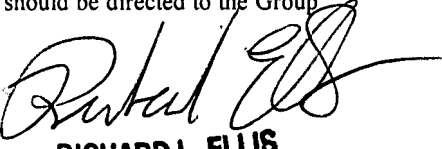
21. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

22. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis  
June 1, 2007

  
**RICHARD L. ELLIS**  
**PRIMARY EXAMINER**